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(54) LIQUID CRYSTAL DISPLAY DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To reduce the frequency of a clock signal to be transmitted to a drive means without increasing the bus width of bus line of display data by generating a multiplied clock signal whose frequency is multiplied based on plural clock signals having the same frequency and phases different from each other.

SOLUTION: A display controller 110 outputs the display data of a simple one column receiving from a main body computer side to drain drivers 130 through the bus line 134 of the display data when a display timing signal is inputted. At this time, the display controller 110 outputs a first clock signal D3 and a second clock signal D4 having the same frequency as that of the first clock signal D3 and the phase different from that of the clock signal D3 to the drain drivers 130 through signal lines 131, 132. The logic circuit parts of the drain drivers 130 generate display data latching clock signal D2 of the frequency double of the frequency of the clock signals (D3, D4) from the clock signal

D3 and clock signal D4.

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CLAIMS

[Claim(s)]

[Claim 1] While sending out the indicative data inputted as the liquid crystal display panel which has two or more pixels formed in the shape of a matrix, and the driving means which impresses the image electrical potential difference based on an indicative data to two or more pixels of the direction of a train to said driving means In the liquid crystal display possessing the display-control means which generates the control signal which includes a clock signal at least based on the input display-control signal inputted, sends out the control signal concerned to said driving means, and carries out the control drive of said driving means Said display-control means has a the same frequency, and two or more clock signals with which phases differ mutually are sent out to said driving means. Said driving means A clock signal multiplying means to generate the multiplying clock signal with which multiplying of the frequency was carried out based on two or more clock signals with which said frequency is the same with clock signals and phases differ mutually, The liquid crystal display characterized by providing at least a storing means to store the indicative data sent out from said display-control means based on the multiplying clock signal generated with said clock signal multiplying means.

[Claim 2] The PURIRATCHI section which stores the indicative data sent out from said display-control means synchronizing with the time of falling of the multiplying clock signal by which said storing means was generated with said clock signal multiplying means (at or the time of a standup), The shift register section which generates a data incorporation signal synchronizing with the time of the standup of the multiplying clock signal generated with said clock signal multiplying means (at or the time of falling), The liquid crystal display indicated by claim 1 characterized by providing at least the input latch section which stores the indicative data outputted from said PURIRATCHI section by the data incorporation signal generated in said shift register section.

[Claim 3] Said display control sends out an indicative data to said driving means through two bus lines. Said storing means It synchronizes at the time of falling of the multiplying clock signal generated with said clock signal multiplying means. The 1st PURIRATCHI section which stores one indicative data of two indicative datas sent out from said display-control means, It synchronizes at the time of the standup of the multiplying clock signal generated with said clock signal multiplying means. The 2nd PURIRATCHI section which stores the indicative data of another side of two indicative datas sent out from said display-control means, The 1st shift register section which generates the 1st data incorporation signal synchronizing with the time

of the standup of the multiplying clock signal generated with said clock signal multiplying means, The 2nd shift register section which generates the 2nd data incorporation signal synchronizing with the time of falling of the multiplying clock signal generated with said clock signal multiplying means, The indicative data outputted from said 1st PURIRATCHI section by the 1st data incorporation signal generated in said 1st shift register section is stored. Moreover, the liquid crystal display indicated by claim 1 characterized by providing at least the input latch section which stores the indicative data outputted from said 2nd PURIRATCHI section by the 2nd data incorporation signal generated in said 2nd shift register section.

[Claim 4] Said two or more clock signals are the liquid crystal displays indicated by any 1 term of claim 1 characterized by being the 2nd clock signal with which the 1st clock signal and said 1st clock signal differ from a phase thru/or claim 3.

[Claim 5] Said clock signal multiplying means is the liquid crystal display indicated by claim 4 characterized by consisting of OR circuits into which the NOR circuit where the AND circuit where said the 1st clock signal and said 2nd clock signal are inputted, and said the 1st clock signal and said 2nd clock signal are inputted, and said AND circuit and said NOR circuit are inputted.

[Claim 6] While sending out the indicative data inputted as the liquid crystal display panel which has two or more pixels formed in the shape of a matrix, and the driving means which impresses the image electrical potential difference based on an indicative data to two or more pixels of the direction of a train to said driving means In the liquid crystal display possessing the display-control means which generates the control signal which includes a clock signal at least based on the input display-control signal inputted, sends out the control signal concerned to said driving means, and carries out the control drive of said driving means Said display-control means has the 1st the same clock signal, said 1st clock signal, and frequency, and sends out the 2nd clock signal with which phases differ to said driving means. Said driving means The 1st PURIRATCHI section which stores the indicative data sent out from said display-control means synchronizing with the time of the standup of said 1st clock signal, The 2nd PURIRATCHI section which stores the indicative data sent out from said display-control means synchronizing with the time of falling of said 1st clock signal, The 1st shift register section which generates the 1st data incorporation signal synchronizing with the time of the standup of said 2nd clock signal, The 2nd shift register section which generates the 2nd data incorporation signal synchronizing with the time of falling of said 2nd clock signal, The indicative data outputted from the 1st PURIRATCHI section by the 1st data incorporation signal generated in said 1st shift

register section is stored. Moreover, the liquid crystal display characterized by providing at least the input latch section which stores the indicative data outputted from the 2nd PURIRATCHI section by the 2nd data incorporation signal generated in said 2nd shift register section.

[Claim 7] The liquid crystal display indicated by any 1 term of claim 1 to which phase contrast (theta) of two or more clock signals with which said frequency is the same with clock signals and phases differ mutually is characterized by being 0< theta<pi or pi<theta<2pi thru/or claim 6.

[Claim 8] The liquid crystal display monitor which is a liquid crystal display monitor equipped with the liquid crystal display indicated by claim 1 thru/or claim 7, and is characterized by inputting said indicative data and an input display-control signal into said display control from the body side of a computer by the signal of a differential format with low amplitude.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] With respect to a liquid crystal display, especially this invention is applied to high resolution-ization of a liquid crystal display panel, and relates to an effective technique.

[0002]

[Description of the Prior Art] A liquid crystal display is divided roughly into the simple MATORISUKU form liquid crystal display which drives the pixel of the intersection of stripe-like XY electrode, and the active matrix liquid crystal display which has an active element (for example, thin film transistor) for every pixel, and carries out the switching drive of this active element.

[0003] The liquid crystal display module of the TFT method equipped with a liquid crystal display panel (TFT-LCD), the drain driver arranged at the liquid crystal display panel bottom, the gate driver arranged on the side face of a liquid crystal display panel, and the interface section as this active matrix liquid crystal display is known.

[0004] In the liquid crystal display module of this TFT method, said liquid crystal display panel has two or more pixels formed in the shape of a matrix, and each pixel has a thin film transistor.

[0005] The drain electrode of the thin film transistor in each pixel of the direction of a train is connected to a drain signal line, respectively, and each drain signal line is connected to the drain driver which impresses an image electrical potential difference (indicative-data electrical potential difference) to the liquid crystal of the pixel of the direction of a train.

[0006] Moreover, the gate electrode of the thin film transistor in each pixel of a line writing direction is connected to a gate signal line, respectively, and each gate signal line is connected to the gate driver which supplies forward bias voltage or negative bias voltage to the gate of 1 horizontal-scanning time amount and a thin film transistor.

[0007] moreover, the liquid crystal display module of this TFT method -- being, the interface section consists of a display control and a power circuit. A power circuit generates the driver voltage impressed to the common electrode of a drain driver, a gate driver, and a liquid crystal display panel.

[0008] A display control consists of one semiconductor integrated circuit (LSI), and controls and drives a drain driver and a gate driver based on the clock signal transmitted from a main-frame-computer side, a display timing signal, a Horizontal Synchronizing signal, each display-control signal of a Vertical Synchronizing signal, and the data for a display.

[0009] A drain driver latches the data for a display to the input register section by the output number based on the clock signal for an indicative-data latch (D2) (a clock signal (D2) is called hereafter.) sent out from a display control. Moreover, based on the clock signal for output timing control (D1) sent out from a display control, the indicative data latched to the input register section is latched to the storage latch

section, and the image electrical potential difference corresponding to each indicative data latched to the storage latch section concerned is further outputted to each drain signal line (D) of a liquid crystal display panel.

[0010] two or more thin film transistors (TFT) connected to each gate signal line (G) of a liquid crystal display panel synchronizing with the clock signal (G1) based on the frame start indication signal and clock signal (G1) with which a gate driver is sent out from a display control -- 1 water -- time of peace -- a sequential flow is carried out for every between.

[0011] An image is displayed on a liquid crystal display panel by the above actuation. In addition, such a technique is indicated by Japanese Patent Application No. No. 247659 [eight to].

[0012]

[Problem(s) to be Solved by the Invention] In the liquid crystal display, high resolution-ization of a liquid crystal display panel is demanded from the former, and the resolution of a liquid crystal display panel has been expanded with 800x600 pixels of a SVGA display mode from 640x480 pixels of for example, a VGA display mode.

[0013] However, in the liquid crystal display, 1600x1200 pixels and the further high-resolution-izing of 1024x768 pixels of an XGA display mode, 1280x1024 pixels of a SXGA display mode, and a UXGA display mode are demanded as resolution of a liquid crystal display panel with the demand of big-screen-izing of a liquid crystal display panel in recent years.

[0014] The display control, the drain driver, and the gate driver are also obliged to high-speed operation with such high-resolution-izing of a liquid crystal display panel, and especially the clock frequency of the clock signal (D2) outputted to a drain driver from a display control and the data for a display has the large effect of improvement in the speed.

[0015] for example, by the 640x480-pixel liquid crystal display panel of a VGA display mode A clock signal (D2) with a frequency of 25MHz and the data for a display with a frequency of 12.5MHz (25MHz one half), moreover, by the 800x600-pixel liquid crystal display panel of a SVGA display mode That they were a clock signal (D2) with a frequency of 40MHz and data for a display with a frequency of 20MHz (40MHz one half) By the 1024x768-pixel liquid crystal display panel of an XGA display mode, a clock signal (D2) with a frequency of 65MHz and the data for a display with a frequency of 32.5MHz (65MHz one half) are needed.

[0016] However, although the data for a display whose frequency is 32.5MHz have been recognized by the drain driver, said clock signal (D2) has not recognized the

clock signal (D2) whose frequency is 65MHz by the drain driver on the relation sent out from a display control to a drain driver through the signal line prepared in a printed-circuit board.

[0017] When transmitting the clock signal (D2) whose frequency is 65MHz on the distributed constant track of this termination disconnection, it becomes remarkable, and waveform distortion is a drain driver and it becomes impossible that is, to recognize a clock signal (D2), although the signal line prepared in a printed-circuit board is equivalent to the distributed constant track of termination disconnection.

[0018] Thus, in the conventional liquid crystal display, when the liquid crystal display panel of high resolution was used with big-screen-izing of a liquid crystal display panel, there was a trouble that the clock signal (D2) of high frequency could not be transmitted to a drain driver from a display control.

[0019] Made in order that this invention may solve the trouble of said conventional technique, the purpose of this invention is in a liquid crystal display to offer the technique which becomes possible [reducing the frequency of the clock signal sent out to a driving means], without increasing the bus width of face of the bus line of an indicative data.

[0020] Without using the delay circuit which is not suitable in the driving means at a special circuit or high-speed operation in a liquid crystal display, other purposes of this invention make a circuit change within a driving means the minimum, and the frequency is in offering the technique which becomes possible [generating the clock signal by which multiplying was carried out] from the clock signal sent out to a driving means.

[0021] Said purpose of this invention and the new description will become clear by description and the accompanying drawing of this specification.

[0022]

[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.

[0023] While sending out the indicative data inputted as the liquid crystal display panel which has two or more pixels formed in the shape of a matrix, and the driving means which impresses the image electrical potential difference based on an indicative data to two or more pixels of the direction of a train to said driving means In the liquid crystal display possessing the display-control means which generates the control signal which includes a clock signal at least based on the input display-control signal inputted, sends out the control signal concerned to said driving means, and carries out the control drive of said driving means Said display-control means has a the same

frequency, and two or more clock signals with which phases differ mutually are sent out to said driving means. Said driving means A clock signal multiplying means to generate the multiplying clock signal with which multiplying of the frequency was carried out based on two or more clock signals with which said frequency is the same with clock signals and phases differ mutually, A storing means to store the indicative data sent out from said display-control means based on the multiplying clock signal generated with said clock signal multiplying means is provided.

[0024] The PURIRATCHI section which stores the indicative data sent out from said display-control means synchronizing with the time of falling of the multiplying clock signal by which said storing means was generated with said clock signal multiplying means (at or the time of a standup), The shift register section which generates a data incorporation signal synchronizing with the time of the standup of the multiplying clock signal generated with said clock signal multiplying means (at or the time of falling), The input latch section which stores the indicative data outputted from said PURIRATCHI section by the data incorporation signal generated in said shift register section is provided.

[0025] Said display control sends out an indicative data to said driving means through two bus lines. Said storing means It synchronizes at the time of falling of the multiplying clock signal generated with said clock signal multiplying means. The 1st PURIRATCHI section which stores one indicative data of two indicative datas sent out from said display-control means, It synchronizes at the time of the standup of the multiplying clock signal generated with said clock signal multiplying means. The 2nd PURIRATCHI section which stores the indicative data of another side of two indicative datas sent out from said display-control means, The 1st shift register section which generates the 1st data incorporation signal synchronizing with the time of the standup of the multiplying clock signal generated with said clock signal multiplying means, The 2nd shift register section which generates the 2nd data incorporation signal synchronizing with the time of falling of the multiplying clock signal generated with said clock signal multiplying means, The indicative data outputted from said 1st PURIRATCHI section by the 1st data incorporation signal generated in said 1st shift register section is stored. Moreover, the input latch section which stores the indicative data outputted from said 2nd PURIRATCHI section by the 2nd data incorporation signal generated in said 2nd shift register section is provided.

[0026] Said two or more clock signals are the 2nd clock signal with which the 1st clock signal and said 1st clock signal differ from a phase.

[0027] Said clock signal multiplying means consists of OR circuits into which the NOR

circuit where the AND circuit where said the 1st clock signal and said 2nd clock signal are inputted, and said the 1st clock signal and said 2nd clock signal are inputted, and said AND circuit and said NOR circuit are inputted.

[0028] While sending out the indicative data inputted as the liquid crystal display panel which has two or more pixels formed in the shape of a matrix, and the driving means which impresses the image electrical potential difference based on an indicative data to two or more pixels of the direction of a train to said driving means In the liquid crystal display possessing the display-control means which generates the control signal which includes a clock signal at least based on the input display-control signal inputted, sends out the control signal concerned to said driving means, and carries out the control drive of said driving means Said display-control means has the 1st the same clock signal, said 1st clock signal, and frequency, and sends out the 2nd clock signal with which phases differ to said driving means. Said driving means The 1st PURIRATCHI section which stores the indicative data sent out from said display-control means synchronizing with the time of the standup of said 1st clock signal, The 2nd PURIRATCHI section which stores the indicative data sent out from said display-control means synchronizing with the time of falling of said 1st clock signal, The 1st shift register section which generates the 1st data incorporation signal synchronizing with the time of the standup of said 2nd clock signal, The 2nd shift register section which generates the 2nd data incorporation signal synchronizing with the time of falling of said 2nd clock signal, The indicative data outputted from the 1st PURIRATCHI section by the 1st data incorporation signal generated in said 1st shift register section is stored. Moreover, the input latch section which stores the indicative data outputted from the 2nd PURIRATCHI section by the 2nd data incorporation signal generated in said 2nd shift register section is provided.

[0029] Said frequency is the same and the phase contrast (theta) of two or more clock signals with which phases differ mutually is 0< theta<pi or pi<theta<2pi.

[0030]

[Embodiment of the Invention] Hereafter, the gestalt of this invention operation is explained with reference to a drawing.

[0031] In addition, in the complete diagram for explaining the gestalt of implementation of invention, what has the same function attaches the same sign, and explanation of the repeat is omitted.

[0032] [Gestalt 1 of implementation of invention] drawing 1 is the block diagram showing the outline configuration of the liquid crystal display module of the TFT method which is the gestalt of 1 operation of this invention.

[0033] The drain driver 130 is arranged at the liquid crystal display panel (TFT-LCD) 10 bottom, and, as for the liquid crystal display module of the gestalt of this operation, a gate driver 140 and the interface section 100 are arranged on the side face of the liquid crystal display panel 10.

[0034] The interface section 100 is mounted in an interface substrate, and is mounted in the printed circuit board of respectively dedication of the drain driver 130 and a gate driver 140.

[0035] Drawing 2 is drawing showing the equal circuit of an example of the liquid crystal display panel 10 shown in drawing 1 .

[0036] As shown in this drawing, the liquid crystal display panel 10 has two or more pixels formed in the shape of a matrix. Each pixel is arranged in the crossover field of two adjoining signal lines (a drain signal line (D) or gate signal line (G)) and two adjoining signal lines (a gate signal line (G) or drain signal line (D)).

[0037] Since each pixel has a thin film transistor (TFT), the source electrode of the thin film transistor (TFT) of each pixel is connected to a pixel electrode (not shown) and a liquid crystal layer is prepared between a pixel electrode and a common electrode (Vcom), between the source electrode of a thin film transistor (TFT), and a common electrode, liquid crystal capacity (CLC) is connected equivalent.

[0038] Moreover, addition capacity (CADD) is connected with the source electrode of a thin film transistor (TFT) between the gate signal lines (G) of the preceding paragraph.

[0039] Drawing 3 is drawing showing the equal circuit of other examples of the liquid crystal display panel 10 shown in drawing 1 .

[0040] In the example shown in drawing 2 , although addition capacity (CADD) is formed between the gate signal line (G) of a whole page, and the source electrode, in the equal circuit of the example shown in drawing 3 , it differs in that retention volume (CSTG) is formed between the common signal line (COM) and the source electrode.

[0041] Although it is applicable to both, since this invention does not have diving in the latter method to the gate signal line (G) pulse of a whole page jumping into a pixel electrode through addition capacity (CADD), the better display of it is attained by the former method.

[0042] In the liquid crystal display panel 10 shown in drawing 2 or drawing 3 , the drain electrode of the thin film transistor (TFT) of each pixel arranged in the direction of a train is connected to a drain signal line (D), respectively, and each drain signal line (D) is connected to the drain driver 130 which impresses an image electrical potential difference (indicative-data electrical potential difference) to the liquid crystal of the

pixel arranged in the direction of a train.

[0043] Moreover, the gate electrode of the thin film transistor (TFT) in each pixel arranged at the line writing direction is connected to a gate signal line (G), respectively, and each gate signal line (G) is connected to the gate driver 140 which supplies forward bias voltage or negative bias voltage to the gate of 1 horizontal-scanning time amount and a thin film transistor (TFT).

[0044] Here, the liquid crystal display panel 10 shown in drawing 1 consists of 1024x3x768 pixels.

[0045] the liquid crystal display module shown in drawing 1 -- being, the interface section 100 consists of a display control 110 and a power circuit 120.

[0046] A display control 110 consists of one semiconductor integrated circuit (LSI), and controls and drives the drain driver 130 and a gate driver 140 based on each display-control signal and the data (R-G-B) for a display of the clock signal (CK) transmitted from a main-frame-computer side, a display timing signal (DTMG), a Horizontal Synchronizing signal (Hsync), and a Vertical Synchronizing signal (vsync).

[0047] A power circuit 120 consists of the forward electrical-potential-difference generation circuit 121, the negative electrical-potential-difference generation circuit 122, a common electrode (counterelectrode) electrical-potential-difference generation circuit 123, a gate electrode voltage generation circuit 124, and a multiplexer 125.

[0048] The forward electrical-potential-difference generation circuit 121 and the negative electrical-potential-difference generation circuit 122 consist of series resistance partial pressure circuits, respectively, and generate the gradation reference voltage of a forward electrical potential difference, or the gradation reference voltage of a negative electrical potential difference.

[0049] According to the alternating current-ized signal (alternating current-ized timing signal;M) from a display control 110, a multiplexer 125 changes the output voltage from the forward electrical-potential-difference generation circuit 121 or the negative electrical-potential-difference generation circuit 122, and outputs it to the drain driver 130.

[0050] The common electrode voltage generation circuit 123 generates the driver voltage (forward bias voltage and negative bias voltage) to which the gate electrode voltage generation circuit 124 impresses the driver voltage impressed to a common electrode to the gate of a thin film transistor (TFT).

[0051] Drawing 4 is the block diagram showing the outline configuration of the drain driver 130 of the gestalt of this operation.

[0052] As shown in this drawing, the drain driver 130 has the electrical-potential-difference generation section 155 for a liquid crystal drive which has the logical circuit section 151, the shift register section 152, the PURIRATCHI section 153, the input latch section 154, and the storage latch section 156, the gradation electrical-potential-difference generation circuit 157, and the electrical-potential-difference bus 158.

[0053] The gradation electrical-potential-difference generation circuit 157 generates the gradation electrical potential difference for 64 gradation based on the gradation reference voltage inputted from the forward electrical-potential-difference generation circuit 121 or the negative electrical-potential-difference generation circuit 122, and outputs it to the electrical-potential-difference generation section 155 for a liquid crystal drive through the electrical-potential-difference bus line 158.

[0054] Drawing 5 is drawing showing the timing chart of the control signal generated with the display-control signal and display control 110 from the main-frame-computer side shown in drawing 1 , and drawing 6 is drawing showing the timing chart of a clock signal (D2) in the clock signal (D3, D4) shown in drawing 5 , and drawing 4 .

[0055] Hereafter, horizontal actuation of the liquid crystal display panel 10 shown in drawing 1 is explained using drawing 4 , drawing 5 , and drawing 6 .

[0056] If a display timing signal is inputted, a display control 110 will judge this to be a display starting position, and will output the indicative data of simple 1 train received from the main-frame-computer side to the drain driver 130 through the bus line 134 of an indicative data. In this case, an indicative data makes one group each data of a 1-pixel unit (R), i.e., red, green (G), and blue (B), and transmits it for every unit time amount.

[0057] In that case, a display control 110 has the 1st the same clock signal (D3) (a clock signal (D3) is called hereafter.) and clock signal (D3), and frequency, and outputs the 2nd clock signal (D4) (a clock signal (D4) is called hereafter.) with which phases differ to the drain driver 130 through a signal line (131,132). In this case, as shown in drawing 6 , the phase of the 2nd clock signal (D4) is delayed for the 1st clock signal (D3) (pi/2).

[0058] In addition, this clock signal (D3) and clock signal (D4) can generate a circuit as shown in drawing 7 easily by having in a display control 110.

[0059] In addition, in the circuit shown in drawing 7 , synchronizing with the time of the standup of the clock signal (CK) from a main-frame-computer side, a clock signal (D3) (or clock signal (D4)) is outputted from the D form flip-flop circuit 111, and a clock signal (D4) (or clock signal (D3)) is outputted from the D form flip-flop circuit 112

synchronizing with the time of the standup of a clock signal (CK) reversal clock signal (at the time of falling of a clock signal (D3)).

[0060] The logical circuit section 151 consists of OR circuits 53 into which NOR circuit 52 where AND circuit 51 where a clock signal (D3) and a clock signal (D4) are inputted, and a clock signal (D3) and a clock signal (D4) are inputted, and AND circuit 51 and NOR circuit 52 are inputted.

[0061] The logical circuit section 151 generates the clock signal for an indicative-data latch (D2) (a clock signal (D2) is called hereafter.) twice the frequency of the frequency of a clock signal (D3) and a clock signal (D4) to a clock signal (D3, D4), as shown in drawing 6 .

[0062] Synchronizing with the time of the standup of the clock signal (D2) from the logical circuit section 151, the shift register section 152 generates the signal for data incorporation of the input latch section 154, and outputs it to the input latch section 154.

[0063] The indicative data from a display control 110 is first inputted into the PURIRATCHI section 153, and the PURIRATCHI section 153 latches an indicative data synchronizing with the time of the standup of the reversal clock signal of a clock signal (D2) (at the time of falling of a clock signal (D2)).

[0064] The input latch section 154 latches the every color bits [6 bits] indicative data from the PURIRATCHI section 110 by the output number synchronizing with a clock signal (D2) based on the signal for data incorporation outputted from the shift register section 152.

[0065] In this case, it was inputted into the carry input of the drain driver 130 of the next step as it is, data latch actuation of the drain driver 130 was controlled by this carry signal, and the carry output of the preceding paragraph of the drain driver 130 has prevented that the mistaken indicative data is written in the data latch section.

[0066] A display control 110 moreover, by counting the clock signal of a predetermined number, after a display timing signal is inputted [whether the input of a display timing signal was completed, and] It judges whether after the display timing signal was inputted, predetermined fixed time amount passed. Or by this As what the indicative data for one horizontal ended, a signal line 133 is minded and it is a clock signal for output timing control (D1) (a clock signal (D1) is called hereafter.) to the drain driver 130. It outputs.

[0067] The storage latch section 156 of the electrical-potential-difference generation section 155 for a liquid crystal drive latches the indicative data in all the input register circuits 156 according to the clock signal (D1) from a display control 110.

[0068] The electrical-potential-difference generation section 155 for a liquid crystal drive chooses one in the gradation electrical potential difference of 64 gradation inputted through the electrical-potential-difference bus line 158 based on the indicative data and alternating current-ized signal (M) which were incorporated by the storage latch section 155, and outputs it to a drain signal line (D).

[0069] Next, actuation of the perpendicular direction of the liquid crystal display panel 10 shown in drawing 1 is explained using drawing 5 .

[0070] If the 1st display timing signal is inputted after a Vertical Synchronizing signal input, a display control 110 will judge this to be 1st display Rhine, and will output a frame start indication signal to a gate driver 140 through a signal line 142.

[0071] Furthermore, a display control 110 outputs the shift clock signal (G1) (a clock signal (G1) is called hereafter.) for making sequential selection of each gate signal line (G) of the liquid crystal display panel 10 to a gate driver 140 through a signal line 141 based on a Horizontal Synchronizing signal for every 1 horizontal-scanning time amount.

[0072] A gate driver 140 is a well-known simple shift scan driver conventionally. two or more thin film transistors (TFT) by which the gate driver 140 was connected to each gate signal line (G) of the liquid crystal display panel 10 synchronizing with the clock signal (G1) based on the clock signal (G1) inputted from a display control 110 when the frame start indication signal (or carry signal of the preceding paragraph) was inputted -- 1 water -- time of peace -- a sequential flow is carried out for every between.

[0073] Generally, when the electrical potential difference (direct current voltage) same for a long time is impressed, the inclination of a liquid crystal layer will be fixed, and a liquid crystal layer will cause an after-image phenomenon as a result, and will contract the life of a liquid crystal layer.

[0074] In order to prevent this, in the liquid crystal display module of the conventional TFT method, itis [alternating-current-] made toize driver voltage impressed to a liquid crystal layer for every (**** is every frame the whole line) fixed time amount of a certain, therefore a display control 110 outputs the alternating current-ized signal (M) for alternating-current-izing driver voltage impressed to a liquid crystal layer for every fixed time amount of a certain to a power circuit 120.

[0075] here, with alternating current-ization, the gradation reference voltage inputted into the drain driver 130 on the basis of the driver voltage of a common electrode (counterelectrode), i.e., the driver voltage impressed to the pixel electrode of a liquid crystal layer, is changed to negative forward electrical-potential-difference side /

electrical-potential-difference side for every fixed time amount -- thing semantics is carried out.

[0076] According to the gestalt of this operation, the 32.5MHz clock signal (D3, D4) which is the same frequency as the frequency of an indicative data is transmitted to the drain driver 130. Thus, in the drain driver 130 interior Since the frequency generated the clock signal for an indicative-data latch (D2) which is 65MHz It becomes possible from a display control 110 to transmit the clock signal (D3, D4) for latching an indicative data to the drain driver 130, without expanding the bus width of face of the bus line 134 of an indicative data.

[0077] Drawing 8 and drawing 9 are the block diagrams showing an example of technique which transmits the clock signal for the indicative-data latch of high frequency (D2) to the drain driver 130 from a display control 110, when the resolution of the liquid crystal display panel examined by this invention person in front of the gestalt of this operation is 1024x768 pixels.

[0078] As a bus line of an indicative data, the approach shown in drawing 8 prepares two bus lines of 134a and 134b, connects the two bus lines (134a, 134b) concerned to each drain driver 130, respectively, and inputs the indicative data for 2 pixels into the drain driver 130.

[0079] Moreover, as a bus line of an indicative data, the approach shown in drawing 9 prepares two bus lines of 134a and 134b, connects the drain driver 130 to the two bus lines (134a, 134b) concerned by turns, and controls two drain drivers 130 to coincidence.

[0080] each approach shown in said drawing 8 and drawing 9 prepares two bus lines (134a, 134b) as a bus line of an indicative data (namely, the bus width of face of the bus line of an indicative data -- twice -- carrying out), sets the frequency of the clock signal for an indicative-data latch (D2) to 32.5MHz (65MHz one half), and transmits the clock signal for an indicative-data latch (D2) to the drain driver 130 from a display control 110.

[0081] However, the approach shown in said drawing 8 and drawing 9 Since the bus width of face of the bus line of an indicative data doubles (for example, if it is 64 gradation and is that of 36 (6x3x2) bit and 256 gradation 48 (8x3x2) bit), The formation of many pins of a display control 110, and multilayering and the formation of area expansion of the printed-circuit board with which the drain driver 130 is carried are caused, and there is a trouble of becoming the factor of a cost rise of the drain driver 130 and a printed-circuit board.

[0082] Furthermore, in the case of 1280x1024 pixels of a SXGA display mode, the

frequency of a clock signal (D2) has it, even if the frequency of 108MHz and an indicative data is set to 54MHz and the resolution of a liquid crystal display panel makes the frequency of a clock signal (D2) one half. [as high-speed as 54MHz]

[0083] Although it can transmit to the drain driver 130 enough from a display control 110 if the frequency of a clock signal (D2) is 27MHz (one half which is 54MHz) In that case, since four bus lines of an indicative data need to prepare and bus-line width of face increases 4 times (for example, if it is 64 gradation and is that of 72 (6x3x4) bit and 256 gradation 96 (8x3x4) bit), The formation of many pins of a display control 110, and multilayering and the formation of area expansion of the printed-circuit board with which the drain driver 130 is carried are caused more, and there is a trouble of becoming the factor of a cost rise of the drain driver 130 and a printed-circuit board.

[0084] Furthermore, the circuitry for distributing an indicative data to two pieces or four bus lines was needed for the display control 110, and there was a trouble the circuitry of a display control 110 not only becomes complicated, but that caused a cost rise.

[0085] However, since what is necessary is just according to the gestalt of this operation not to expand the bus width of face of the bus line of an indicative data, to form the logical circuit section 151 in the drain driver 130, and to add one signal line further for a clock signal (D3) or a clock signal (D4), the formation of many pins of a display control 110, and multilayering and the formation of area expansion of the printed-circuit board with which the drain driver 130 is carried are not caused. Moreover, there are also few cost rises of the drain driver 130 and a printed-circuit board, and they end.

[0086] Moreover, when the resolution of a liquid crystal display panel is 1024x768 pixels, from a display control 110, as other examples of the technique of transmitting the clock signal for an indicative-data latch of high frequency (D2) to the drain driver 130, the frequency of a clock signal (D2) is set to 32.5MHz (65MHz one half), and there is the approach of latching an indicative data in the time of the standup of a clock signal (D2) and falling in the drain driver 130.

[0087] According to this approach, it becomes possible to reduce the frequency of a clock signal (D2) like the approach shown in drawing 8 and drawing 9 , without expanding the bus width of face of the bus line of an indicative data.

[0088] However, the clock signal for an indicative-data latch inputted into the PURIRATCHI section 153 (reversal clock signal of the clock signal (D2) of drawing 1), Between the clock signals for control (clock signal of drawing 1 (D2)) inputted into the shift register section 152 By the approach which needs to secure predetermined

timing in order to prevent the racing of timing, and latches an indicative data in the time of the standup of a clock signal (D2), and falling As the clock signal which consists of a frequency twice the frequency of a clock signal (D2) is generated or it is shown in drawing 10 , it is necessary to carry out predetermined time delay of the clock signal (D2) in a delay circuit 159, and to input it into the shift register section 152 in the drain driver 130 interior.

[0089] In this case, a special circuit is required in order to generate the clock signal which consists of a frequency twice the frequency of a clock signal (D2) from the time of the standup of a clock signal (D2), and falling. Moreover, the design of the time delay of the delay circuit 159 shown in drawing 10 has a large burden because of high speed correspondence.

[0090] Therefore, by the approach of latching an indicative data in the time of the standup of a clock signal (D2), and falling, a special circuit is required for the drain driver 130 interior, or there was a trouble that a burden was large, for high speed correspondence of a design of the time delay of a delay circuit 159.

[0091] However, with the gestalt of this operation, a special circuit is not required for the drain driver 130 interior, and a setup of the time delay of the delay circuit unsuitable for high-speed operation does not have the need, either.

[0092] In addition, in the gestalt of this operation, although the case where the 1st and 2nd clock signals (D3, D4) were used was explained, it is also possible by using n clock signals (D3, D4 .. Dn) from the 1st to the n-th to reduce more the frequency of the clock signal (D3, D4 .. Dn) for latching an indicative data. In that case, the logical circuit section 151 needs to generate the clock signal (D2) carried out n multiplying from n clock signals (D3, D4 .. Dn).

[0093] [Gestalt 2 of implementation of invention] drawing 11 is the block diagram showing the outline configuration of the drain driver 130 of the gestalt of other operations of this invention.

[0094] The drain driver 130 of the gestalt of this operation omits the logical circuit section 151 shown in drawing 4 , and prepares the two PURIRATCHI sections (153a, 153b) and the two shift REJITA sections (152a, 152b).

[0095] Here, PURIRATCHI section 153a latches an indicative data synchronizing with the time of the standup of a clock signal (D3), and PURIRATCHI section 153b latches an indicative data synchronizing with the time of the standup of the reversal clock signal of a clock signal (D3) (at the time of falling of a clock signal (D3)).

[0096] Shift register section 152a outputs the signal for data incorporation synchronizing with the time of the standup of a clock signal (D4), and shift register

section 152b outputs the signal for data incorporation synchronizing with the time of the standup of the reversal clock signal of a clock signal (D4) (at the time of falling of a clock signal (D4)).

[0097] The indicative data which the indicative data latched to PURIRATCHI section 153a was incorporated by the input latch section 154 with the signal for data incorporation from shift register section 152a, and was latched to PURIRATCHI section 153b is incorporated by the input latch section 154 with the signal for data incorporation from shift register section 152b.

[0098] Thus, with the gestalt of this operation, a clock signal (D3) is only used for the PURIRATCHI sections (153a, 153b), and a clock signal (D4) is only used for the shift register sections (152a, 152b).

[0099] Also in the gestalt of this operation, it becomes possible to transmit the KUKUROKKU signal (D3, D4) for latching the indicative data of high frequency to the drain driver 130 from a display control 110, without expanding the bus width of face of the bus line of an indicative data.

[0100] [Gestalt 3 of implementation of invention] drawing 12 is the block diagram showing the outline configuration of the drain driver 130 of the gestalt of other operations of this invention.

[0101] Drawing 13 is drawing showing the timing chart of an indicative data and a clock signal (D3, D4).

[0102] With the gestalt of this operation, as a bus line of an indicative data, two bus lines of indicative-data A and indicative-data B are prepared, and the two PURIRATCHI sections (153a, 153b) and the two shift REJITA sections (152a, 152b) are prepared in the drain driver 130. Here, the frequency of indicative-data A and indicative-data B is the same, and the phase of indicative-data B is delayed for indicative-data A (pi/2).

[0103] PURIRATCHI section 153a latches indicative-data A at the time of the standup of the reversal clock signal of the clock signal (D2) from the logical circuit section 151 (at the time of falling of a clock signal (D2)), and PURIRATCHI section 153b latches indicative-data B synchronizing with the time of the standup of a clock signal (D2).

[0104] Shift register section 152a outputs the signal for data incorporation synchronizing with the time of the standup of a clock signal (D2), and shift register section 152b outputs the signal for data incorporation at the time of the standup of the reversal clock signal of a clock signal (D2) (at the time of falling of a clock signal (D2)).

[0105] Indicative-data B which indicative-data A latched to PURIRATCHI section 153a was incorporated by the input latch section 154 with the signal for data incorporation from shift register section 152a, and was latched to PURIRATCHI section 153b is incorporated by the input latch section 154 with the signal for data incorporation from shift register section 152b.

[0106] In the gestalt of this operation, since two bus lines of an indicative data were prepared, it becomes possible to reduce further the frequency of the clock signal (D3, D4) for latching an indicative data.

[0107] [Gestalt 4 of implementation of invention] drawing 14 is drawing showing the appearance of an example of the liquid crystal display monitor equipment which is the gestalt of other operations of this invention, and drawing 15 is the block diagram showing the outline configuration of the liquid crystal display monitoring device of the gestalt of this operation.

[0108] As for liquid crystal display monitor equipment and 210, in drawing 14 , 200 is [the cable for monitors and 220] the connectors for monitors. The gestalt of this operation is a gestalt of the operation which applied this invention to liquid crystal display monitor equipment, and the digital interface is used for the liquid crystal display monitor equipment 200 of the gestalt of this operation as an interface by the side of the body of a personal computer.

[0109] In the gestalt of this operation, each display-control signal and the data (R-G-B) for a display of a clock signal (CK), a display timing signal (DTMG), a Horizontal Synchronizing signal (Hsync), and a Vertical Synchronizing signal (vsync) are sent out from the body side of a computer by the LVDS (Low Voltage Differential Signaling) method.

[0110] Therefore, as shown in drawing 15 , the transmitter (170a, 170b) and receiver (160a, 160b) which consist of semiconductor integrated circuits (LSI), respectively are formed between the output stage of the graphic controller 180 by the side of the body of a computer, and the input stage of a display control 110.

[0111] The other circuitry is the same as the circuitry shown in drawing 1 . However, since a drawing becomes complicated, the signal line 135 with same signal line of a clock signal (D3) and signal line of a clock signal (D4) expresses in drawing 15 .

[0112] Said transmitter 170a (or 170b) carries out juxtaposition-serial conversion of the 21-bit signal by all of the display timing signal (DTMG) from a graphic controller 180, a Horizontal Synchronizing signal (Hsync), a Vertical Synchronizing signal (vsync), and the data (R-G-B) for a display, and sends it out to receiver 160a (or 160b) with the twisted pair line from those [three].

[0113] Said receiver 160a (or 160b) carries out said serial signal a serial-parallel conversion, and sends out a display timing signal (DTMG), a Horizontal Synchronizing signal (Hsync), a Vertical Synchronizing signal (vsync), and the data (R-G-B) for a display to a display control 110.

[0114] Moreover, a clock signal (CK) is transmitted to receiver 160a (or 160b) from said transmitter 170a (or 170b) with the twisted pair line from that [one].

[0115] Here, the frequency of the serial signal on the twisted pair line is 7 times the frequency of a clock signal (CK) from those [three].

[0116] In addition, with the gestalt of this operation, the interface by the side of the body of a personal computer may be an analog interface, and it cannot be overemphasized in that case that it is necessary to change the video signal of R-G-B of an analog into a digital signal at a liquid crystal display monitor equipment side.

[0117] Moreover, although the gestalt of said the operation of each explained the case where this invention was applied to the liquid crystal display of a TFT method, it is not limited to this and it cannot be overemphasized that this invention can be applied also to the passive-matrix form liquid crystal display of a STN method.

[0118] As mentioned above, although invention made by this invention person was concretely explained based on the gestalt of implementation of said invention, as for this invention, it is needless to say for it to be able to change variously in the range which is not limited to the gestalt of implementation of said invention and does not deviate from the summary.

[0119]

[Effect of the Invention] It will be as follows if the effectiveness acquired by the typical thing among invention indicated in this application is explained briefly.

[0120] (1) It becomes possible to reduce the frequency of the clock signal sent out to a driving means, without increasing the bus width of face of the bus line of an indicative data in the liquid crystal display in which high resolution carries out liquid crystal display panel possession according to this invention.

[0121] (2) Without using a special circuit or a delay circuit into a driving means in the liquid crystal display in which high resolution carries out liquid crystal display panel possession according to this invention, make a circuit change within a driving means the minimum, and the frequency becomes possible [generating the clock signal by which multiplying was carried out] from the clock signal sent out to a driving means.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the block diagram showing the outline configuration of the liquid crystal display module of the TFT method which is the gestalt of 1 operation of this invention.

[Drawing 2] It is drawing showing the equal circuit of an example of the liquid crystal display panel shown in drawing 1 .

[Drawing 3] It is drawing showing the equal circuit of other examples of the liquid crystal display panel shown in drawing 1 .

[Drawing 4] It is the block diagram showing the outline configuration of the drain driver of the gestalt 1 of this operation.

[Drawing 5] It is drawing showing the timing chart of the control signal generated with the display-control signal and display control 110 from the main-frame-computer side shown in drawing 1 .

[Drawing 6] It is drawing showing the timing chart of the clock signal (D2) shown in the clock signal (D3, D4) shown in drawing 5 , and drawing 4 .

[Drawing 7] It is drawing showing an example of the circuitry which generates a clock signal (D3) and a clock signal (D4) with the display control of the gestalt 1 of this operation.

[Drawing 8] When the resolution of the liquid crystal display panel examined by this invention person in front of the gestalt of this operation is large resolution, it is the block diagram showing an example of technique which transmits the clock signal for the indicative-data latch of high frequency (D2) to a drain driver from a display control.

[Drawing 9] When the resolution of the liquid crystal display panel examined by this

invention person in front of the gestalt of this operation is large resolution, it is the block diagram showing an example of technique which transmits the clock signal for the indicative-data latch of high frequency (D2) to a drain driver from a display control.

[Drawing 10] When the resolution of the liquid crystal display panel examined by this invention person in front of the gestalt of this operation is large resolution, it is the block diagram showing the outline configuration of the drain driver which latched the indicative data in the time of the standup of a clock signal (D2), and falling.

[Drawing 11] It is the block diagram showing the outline configuration of the drain driver of the gestalt 2 of this operation.

[Drawing 12] It is the block diagram showing the outline configuration of the drain driver of the gestalt 3 of this operation.

[Drawing 13] It is drawing showing the timing chart of the clock signal (D3, D4) of the gestalt 3 of this operation, and a clock signal (2).

[Drawing 14] It is drawing showing the appearance of an example of the liquid crystal display monitor equipment which is the gestalt of other operations of this invention.

[Drawing 15] It is the block diagram showing the outline configuration of the liquid crystal display monitoring device of the gestalt 4 of this operation.

[Description of Notations]

10 -- A liquid crystal display panel (TFT-LCD), 51 -- An AND circuit, 52 -- NOR circuit, 53 -- An OR circuit, 100 -- The interface section, 110 -- Display control, 111,112 -- A D form flip-flop circuit, 120 -- A power circuit, 121 -- Forward electrical-potential-difference generation circuit, 122 -- A negative electrical-potential-difference generation circuit, 123 -- Common electrode (counterelectrode) electrical-potential-difference generation circuit, 124 -- A gate electrode voltage generation circuit, 125 -- A multiplexer, 130 -- Drain driver, 151 -- The logical circuit section, 152,152a, 152b, 162 -- Shift register section, 153,153a, 153b -- The PURIRATCHI section, 154 -- Input latch section, 155 -- The electrical-potential-difference generation section for a liquid crystal drive, 156 -- The storage latch section, 157 -- Gradation electrical-potential-difference generation circuit, 158 [-- Receiver,] -- An electrical-potential-difference bus, 159 -- A delay circuit, 140 -- A gate driver, 160a, 160b 170a, 170b [-- The cable for monitors, 220 / -- Connector for monitors.] -- A transmitter, 180 -- A graphic controller, 200 -- Liquid crystal display monitor equipment, 210